This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1-21. (canceled).

22-24. (previously withdrawn).

25. (currently amended) A semiconductor package comprising:

a planar low temperature co-fired ceramic substrate having a first and second layer mounted adjacent each other, the first layer having a first surface and the second layer having a second surface,

a micro-machined semiconductor device located adjacent the first surface, the micro-machined semiconductor device having a plurality of first pads and an active central area;

a plurality of ball pads located on the second surface;

a plurality of second pads located on the first surface;

a plurality of vias, extending through the substrate between the first and second surfaces, the vias connected to the ball pads and to the first pads;

a reflowed solder joint located between the first and second pads for electrically connecting the substrate to the semiconductor device, the reflowed solder joint formed from a first reflowed solder paste;

a solder seal ring, located between the micro-machined semiconductor device and the first surface around an outer perimeter of the substrate for making a hermetic seal between the micro-machined semiconductor device and the substrate;

a plurality of ultrasonically deposited wire bond bumps located between the micro-machined semiconductor device and the first surface for supporting the micro-machined semiconductor device during assembly and preventing the micro-machined semiconductor device from contacting the first surface during reflow of the solder joint, the wire bond bumps further spacing the micro-machined semiconductor device from the first surface, the wire bond bumps further arranged around the active area, the wire bond bumps formed from a metal; ~~and~~

a plurality of solder spheres mounted to the ball pads by a second reflowed solder paste; and

wherein the substrate does not have cavity.

26. (previously presented) The semiconductor package according to claim 25, wherein a plurality of circuit lines are located on the first surface, the circuit lines connected between the vias and the second pads.

27. (canceled).

28. (previously presented) The semiconductor package according to claim 25, wherein the wire bond bumps are formed from either gold or an alloy of gold.